THEORY OF OPERATION

1. INTRODUCTION

This section provides a functional description of the radio, presented as follows:

- Receive and transmit paths.
- Electronic boards.
- Control functions.

Refer to the appropriate diagrams while reading the following functional description.

2. RECEIVE AND TRANSMIT PATHS
(See Figure 1)

2.1 RECEIVE PATH

Signals received from the antenna pass to the HF (Harmonic Filter) board (1), where a relay-selected low-pass filter rejects signals above the selected range. An antenna relay switches the HF board between the receive and transmit paths. In the receive mode, the antenna relay switches the signal to a 1.6-to-30 MHz bandpass filter (2) and Front End LPF (3). The output of this filter is passed to an active RF attenuator (4), controlled by the RGC (Receive Gain Control) line originating in the A board.

The attenuated RF signal is transferred to an RF amplifier (5), and then, via a coaxial cable, to the S board.

In the S board the received signal is converted by the first mixer (9) to a 75 MHz IF signal. This signal passes through the 75 MHz IF strip (10), which consists of the 75 MHz IF crystal filter and RF amplifier. The second conversion, to an 11.4 MHz IF signal, is performed by the second mixer (11). The converted signal is applied to the A board via a coaxial cable.

If the converted signal passes through an optional activated noise blanker (12), it is sharply attenuated when a noise spike appears. A bidirectional amplifier (13) amplifies the 11.4 MHz IF signal, and also provides impedance matching for the 11.4 MHz crystal filter (14). The filter passes signals in the upper side of the 11.4 MHz IF signal (the bandwidth for 6 dB attenuation is 350 to 2700 Hz above 11.4 MHz).

The crystal filter (14) is used in both USB and LSB modes. Inserting the desired sideband to the filter is performed by frequency shifting of the second injection signal, and an appropriate shift of the demodulation injection.

The IF signal is transferred from the crystal filter to another bidirectional amplifier stage (15) and then enters the receive IF amplifier stage (16). This last IF stage consists of an active attenuator, a voltage controlled amplifier (both controlled by the RGC line) and a tuned amplifier, whose output is fed to the demodulator (17) and to the RGC detector (20). This detector generates a DC voltage, proportional to the received signal, on the RGC control lines.

The Interconnection board transfers the demodulated (audio) signal to the C board where it is fed through an active filter and an audio amplifier (22) to the loudspeaker (39).

A squelch circuit (25) on the B board generates a squelch signal when no voice is present in the signal received from the A board.

This squelch signal passes to the A board to generate a mute signal. The mute signal disables the audio power amplifier.

2.2 TRANSMIT PATH

The signal to be transmitted may be a speech signal received from a Motorola preamplifier microphone, an external data signal from the AUX connector or a data signal originating inside the radio (i.e., DSC signalization).

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68P02940C88-O
April, 1994

The transmit signal is applied to the audio section of the A board via the Interconnection board.

In the A board the signal is amplified after passing through an active attenuator controlled by the automatic TGC (Transmit Gain Control) circuit. The TGC circuit adjusts the level of the audio signal to an optimum value for the modulator.

The gain controlled audio signal is applied to the modulator (17) (an active double-balanced mixer), where it is mixed with an IF carrier signal (11.4 MHz in LSB mode or 11.403 MHz in USB mode). This signal originates in a PLL hybrid, located on the A board (27).

The output of the modulator is a double-sided, suppressed-carrier signal centered around either 11.4 MHz in LSB mode, or 11.403 MHz in USB mode. Carrier suppression is factory optimized by means of a balancing potentiometer.

The double-sided, suppressed-carrier signal is sent both to the TGC detection circuit and to the transmit portion of the 11.4 MHz IF amplifier (15). The input of this amplifier is controlled by the TGC circuit, which controls the level of the audio signal.

The double-sided, suppressed-carrier signal is amplified and applied to the same crystal filter set (14) used in the receive path. This filter rejects undesired sideband and attenuates the carrier. The single sideband signal is buffered and sent to the S board for mixing with the second injection signal, to a 75 MHz IF signal.

The A board also contains the carrier reinsertion circuit (21). This circuit receives the IF carrier signal from the 11.4 MHz PLL hybrid, attenuates it to the AME or PILOT level, and injects it back to the transmit path after the crystal filters. In this way the carrier appears again: in AME mode it appears 6 dB below PEP (when a single tone is transmitted) and in PILOT mode 18 dB below PEP (when a single tone is transmitted). In SSB mode there is no carrier reinsertion.

The 11.4 MHz IF signal, received from the A board via the coaxial cable, enters the S board in the frequency conversion and 75 MHz IF strip. The first conversion (in the transmit path) is performed by the "second" mixer (11), where the 11.4 MHz IF signal is mixed with a 63.6 MHz signal to produce the 75 MHz IF signal (the 63.6 MHz signal can be varied ±5.625 kHz in 50 Hz steps for fine frequency control). The 75 MHz output from the second mixer is then amplified by the transmit portion of the 75 MHz IF filter (10), and transferred to the first mixer (9), where it is mixed with the first injection signal to produce the output RF signal.

The RF signal is transferred via a coaxial cable to the exciter filter (8) and amplifier (7) located on the B board. The output signal of the B board (which is in the range of +10 to +20 dBm) is amplified to approximately +52 dBm by the final power amplifier unit (6).

The power amplifier unit (6) consists of four stages of linear amplification and various control circuits for output power level control. It also contains protection circuits against high temperature and damaging VSWR conditions.

The RF output signal proceeds to the same harmonic filter (1) used in the receiver path. In transmit mode, the forward and reflected power is detected between the filter and the antenna. The detector produces two DC signals: one proportional to the forward RF power, and the other proportional to the reflected RF power. These DC signals are used as control signals for the power amplifier and for power level indication.

3. ELECTRONIC BOARDS

The circuitry of the basic MICOM·XF radio is composed of seven functional boards, as follows:

- A board.
- B board.
- C board.
- S board.
- Power Amplifier.
- Interconnect board.
- Harmonic Filter board.

Some of the boards perform two or more different functions.

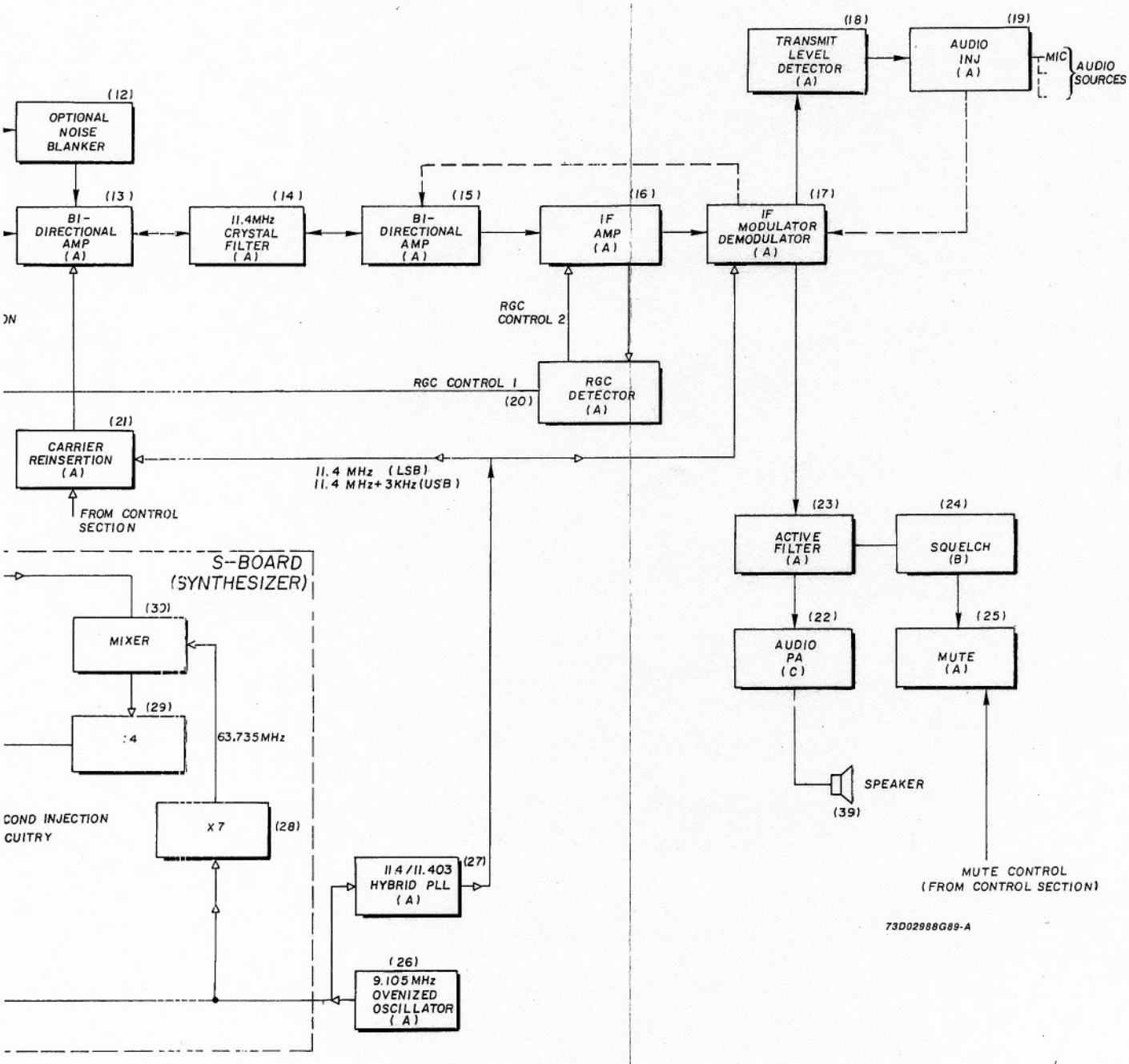
The following subparagraphs describe the content of each board and its main functions. Additional information about circuit operation is provided on the schematic diagrams next to the circuit of interest.

3.1 A BOARD

The main sections of the A board are the 11.4 MHz IF receive and transmit sections and control components.

The receive path of the board consists of an 11.4 MHz amplification chain of approximately 85 dB. The amplification chain is implemented by the following components:

- Dual-transistor amplifier (Q39 and Q40).
- Common base buffer (Q44) and two IC's (U8 and U9).
- Three crystal IF filter elements which determine the bandwidth of the radio (also used in the transmit path).



Block Diagram

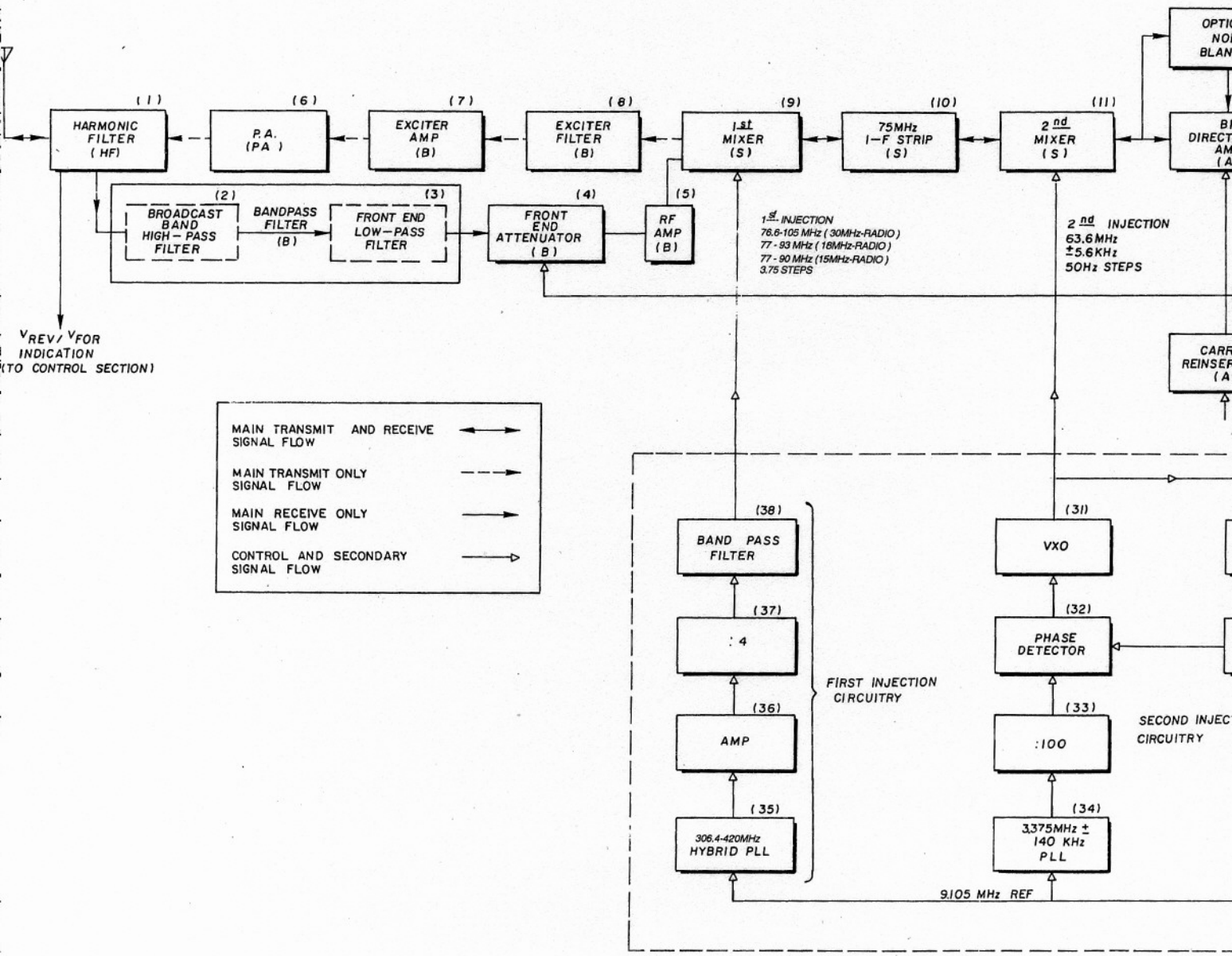


Figure 1. Radio Block D

- Demodulation circuit (U10).
- Active audio filter (Q51).

The receive path also includes an automatic RGC circuit which maintains the output level constant for a large dynamic range of incoming signals.

The transmit path of the A board consists of the following components:

- Audio input amplifier (Q33 and Q34).
- Modulator circuit (U10).
- Automatic TGC and IF buffers and amplifiers.

The carrier reinsertion circuit is also part of the transmit path. It reinjects the 11.4 MHz carrier signal, behind the crystal filter, at the necessary level for AME and PILOT modes.

The A board also contains a 9.105 MHz reference oscillator (Q60 through Q63) and its temperature control circuit (U11, Q58, and Q59). All frequency sources in the radio are derived from this single oven-controlled reference oscillator. Consequently, the radio's overall stability and accuracy are determined by this reference oscillator.

The reference oscillator is kept in an oven, proportionally controlled by electronic circuitry to nominal temperature of 81 °C (refer to U11, Q58, Q59, and peripheral components in the A board drawing). The crystal temperature is kept within the limits of ±2 °C for ambient temperature change of –30 to +60 °C.

The oscillator (Q60, C112 through C115, and Y4) is based on pierce configuration which is the recommended configuration for best short and long time stability. The oscillator's output is amplified by Q61 and then fed to a buffer stage (Q62) to minimize loading effects. In addition, the buffer output is fed to a signal level detector (Q63) – part of the AGC (Automatic Gain Control) loop which controls Q60 gain, maintaining a constant drive level on the crystal. This level stabilization provides optimum drive level to the crystal for minimum aging effects and maximum frequency vs. temperature stability.

The total frequency stability of the reference oscillator (and the radio itself) over the –20 to +50 °C temperature range is better than ±0.3 PPM, equivalent to ±9 Hz at 30 MHz operation.

The 9.105 MHz reference signal is applied to the 11.4 MHz PLL Hybrid (U7) to produce the injection signal for SSB modulation/demodulation. The 9.105 MHz reference signal is also sent to the PLL circuits of the S board.

The A board performs some radio control functions by means of three encoding/decoding ICs (U2, U3, and U5) and two shift registers (U1 and U4). The shift registers hold the status of the control commands which are serially transferred by the SPI line from the radio's control section in the S board. For further details on the A board control functions, refer to paragraph 4 – Control Functions.

The A board also includes two connectors, J22 and J21, for inserting optional IF crystal filter and noise blanker, respectively.

3.2 B BOARD

The B board performs several functions. It includes part of the receive path: a band-pass filter tuned to the reception band (1.6–30 MHz), the first attenuator (Q10) of the automatic RGC system, and the first front end amplifier (Q11 and Q13).

The transmit path circuits of the B board are: band pass filter, wide-band 12 dB amplifier (Q14 and Q15), 28 dB predriver and a control circuit (Q20). The control circuit acts as an automatic level control (ALC), which controls the output power level according to the control signal ALC-ATTN from the power amplifier.

The B board contains the receiver squelch circuit (hybrid). This circuit receives and processes the received audio signal from the A board. When no voice characteristics are identified in the received audio signal, the B board then generates a mute signal, which mutes the audio power amplifier.

The B board also contains regulation and switching circuits which switch ON the 9T supply line and switch OFF the 9R supply line when the PTT line is pulled down. The same circuits switch ON the 9R supply line and switch OFF the 9T supply line when the PTT line is released.

The B board contains the ARQ Interface circuit, that enables fast receive/transmit switchover. The one-shot timer U2 is triggered for approximately 10 ms on each modem transmit-to-receice transition. This pulse drives the blanking transistor Q24 and the muting transistor Q25. Transistor Q24 is in the ON state, thus disabling the RGC Detector operation on the modified A board and decreasing the RGC attenuation to a minimum; at the same time transistor Q25 mutes the audio signal. This ensures that a delay of no more than 15 ms occurs from the rising time of the radio PTT to the point where the received audio reaches 90% of the final value.

When the DATA PTT line drops, it turns transistor Q22 off. After a delay of approximately 10 ms (determined by C104 and R106) transistor Q21 turns on and enables (grounds) the PA INHIBIT line. This operation ensures

that the power rising time during PTT drops, and the point where power reaches 90% of its nominal value is less than 15 ms.

3.3 C BOARD

The C board is located behind the front panel and holds the LCD display. It has three main functions: display control, keyboard decoding and audio amplification.

The display control function is performed by two display control ICs (U2 and U3) which are fed by the control section of the radio.

The keyboard decoding function is performed by an IC decoder (U4). For detailed information on reading the keyboard and writing to the display, refer to paragraphs 4.1.1 and 4.1.2.

The audio signal path on the C board includes audio switching for mute purposes and an audio power amplifier stage implemented by IC TAA2803 (U6).

3.4 INTERCONNECTION BOARD

The Interconnection board is mainly a junction board for the control and audio lines received/transferred from/to the A board, S board, C board, and front panel connectors and controls. This board also includes an IC socket for an optional RS232 level translator IC and potentiometer for adjusting the RF output level in DATA mode.

3.5 HF (HARMONIC FILTER) BOARD

The HF board is used to attenuate the unwanted harmonics of the transmitted and received signals. During transmission, the TX/RX switch is in the Transmit state, transferring the RF output from the power amplifier to the antenna via the HF board. In the receive mode, the TX/RX switch is in the Receive state, transferring the received signal from the antenna to the B Board via the HF board.

The HF board contains the following components:

- Seven selectable low pass filters (see table below).
- Seven electronic switches (see table below), used to select the required low pass filter. Only one switch is open at a time.
- TX/RX electronic switch (CR1, CR2, CR3, CR4, CR27 and CR42).
- Forward/reverse power detector (T1, CR23 and CR24).
- Regulator, including two linear regulators U1 and U2 and accessories.
- High voltage power supply.

Filter	Range (MHz)	Electronic Switch
1	1.6–2.43	CR13, CR14
2	2.43–3.7	CR19, CR20
3	3.7–5.6	CR6, CR15, CR16, CR22
4	5.6–8.5	CR9, CR10
5	8.5–13	CR6, CR11
6	13–19.8	CR17, CR18, CR29, CR30
7	19.8–30	CR5, CR7, CR8, CR21

3.5.1 Functional Description

The HF board contains seven selectable low pass filters, each covering a section of the 1.6 - 30 MHz range. Seven control lines are used to select an appropriate filter according to the operating frequency. When a control line is pulled down, a corresponding PIN diode switch is turned on, selecting and enabling the filter.

A forward/reverse power detector is inserted between the filters and the antenna. During transmission it generates two DC signals. One of these signals is proportional to the forward RF power delivered to the antenna, and the other is proportional to the RF power reflected from the antenna. The signals are sent to the power amplifier for controlling the level of the power output as a function of the following parameters:

- VSWR value. If the VSWR increases above 2:1, the output power is gradually decreased, to protect the radio from high levels of reflected power.
- Harmonic filter insertion losses. If the Harmonic filter insertion losses are too high, the output power level is decreased.

3.5.2 Major Improvements

Each of the low pass filters (LPFs) in the HF board now consists of three toroid inductors and chip capacitors. The utilization of the new types of inductors has significantly decreased inductor radiation on other parts of the radio, and thus enabled an increase in the filter density and decrease in the board size. In addition, the toroid inductors and the chip capacitors significantly improve the radio's reliability.

3.6 PA (POWER AMPLIFIER) BOARD

The PA board operates over 1.6-30 MHz frequency range and contains the following RF wide band amplification stages:

- Push-pull driver (Q16, Q17).
- Final push-pull power stage (Q18 and Q19).

The PA board includes a control circuit which controls the output power level according to the position of the ALC potentiometer (or TUNE potentiometer during tune operation), the temperature of the final push-pull transistors case, and the VSWR that the radio faces. This circuit is implemented by three current operational amplifiers (U1), which receive the abovementioned inputs. It controls an active attenuator (located on the B board), which regulates the RF input to the amplification stages.

A four-transistor latch circuit compares the power obtained from the forward power detect circuit in the harmonic filter, with a sample of the output power from the final amplifiers. If the output power from the harmonic filter is less than 60% of the final amplifier output power, the latch circuit causes to shunt input RF power to ground (by activating the ALC attenuator on the B board), eliminating the RF power at the output.

A two-transistor circuit (Q2, Q11) controls the bias of the driver and final amplifier transistors; as heat-sink temperature increases, the circuit reduces the bias correspondingly.

3.7 S BOARD

The S board contains the following three circuits:

- Frequency synthesizer.
- 75 MHz IF.
- Control section of the radio.

In order to ease the understanding of the frequency synthesizer structure and operation, the description in the following paragraph is more detailed.

3.7.1 Frequency Synthesizer

The frequency synthesizer components are located on the S board in four compartments – see Figure 2. The main function of the frequency synthesizer is to generate the injection signals which are fed to the first (9) and second (11) mixers. The synthesizer is controlled by the control section of the radio, located in the S board.

NOTES

1. For a better understanding of the frequency synthesizer description, see Figure 1 – Radio block diagram.
2. The numbers in parenthesis refer to the Radio block diagram.

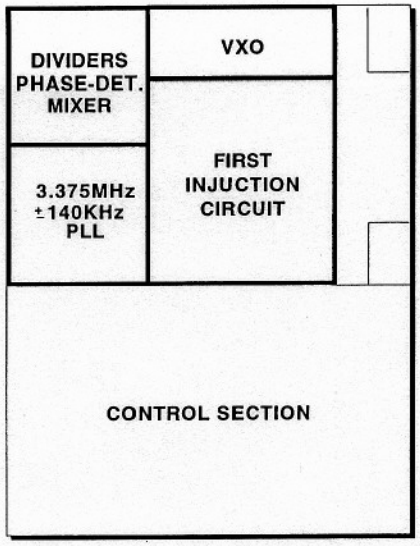


Figure 2. Frequency Synthesizer Components Location

3.7.1.1 First Injection Circuit

The first injection signal is generated by the PLL hybrid (35) and divided by 4 (37) before it is injected into the first mixer. The PLL hybrid (35) consists of a phase locked loop with programmable divider. The divider generates signals in the range of 306.4 to 420 MHz in 15 kHz steps. The PLL hybrid includes two VCOs to provide such wide variation; the first VCO covers the range of 306.4 to 357 MHz and the second VCO covers the range of 357 to 420 MHz.

The output signal of the PLL hybrid is amplified and fed into a divider-by-4 (U2). The divider outputs a signal in the range of 76.6 to 105 MHz in 3.75 kHz steps. The divider output signal passes through a final amplification stage and a bandpass filter (38) before being applied to the input of the mixer.

Various voltages are applied to the first injection circuit. Some of them are applied via regulators and DC filters for stabilization and noise rejection. Some of the power supply circuits are located in the control section, including a voltage doubler circuit which generates the 2SWA voltage.

3.7.1.2 Second Injection Circuit

The second injection circuit generates the second injection signal (63.6 MHz ±5.6 kHz in 50 Hz steps). A double loop is used for achieving 50 Hz resolution, and relatively fast lock time, with good reference rejection. The first loop (34) includes a PLL with a programmable divider, which generates a signal in the range of 3.375 MHz ±140 kHz in 1.25 kHz steps. The output of this loop is fed via appropriate amplification and

buffering to a divider-by–100. The divider output is used as a reference frequency for the final loop.

The 3.375 MHz ±140 kHz signal (in 1250 Hz steps) is applied to the phase detector of the final loop (32). The output of the phase detector drives a voltage-controlled crystal oscillator (VXO) which generates the output frequency of 63.6 MHz ±5.6 kHz in 50 Hz steps. The final loop is closed via an active mixer (30) and a divider-by-4 (29).

The second input of the mixer is fed with a 63.735 MHz signal, generated by multiplying the 9.105 MHz reference frequency by 7. The difference between the frequencies of both inputs is applied to the divider-by-4 and then to the second input of the phase detector. The divider-by-100, divider-by-4, and the phase comparator are integrated into one integrated circuit (MC14568-U22).

3.7.2 75 MHz IF Circuit

The 75 MHz IF circuit serves the receive and transmit paths. Some of the elements of this circuit are bidirectional and are used by the receive and transmit paths. The 75 MHz IF circuit includes two mixers. The first mixer (U14) converts received signals in the 1.6-30 MHz range to 75 MHz in receive mode; in transmit mode, the 75 MHz IF signal is converted to a signal in the 1.6–30 MHz range. The second mixer (U15) converts the 75 MHz IF signal to 11.4 MHz signal in receive mode; in transmit mode, the 11.4 MHz signal is converted to 75 MHz IF signal.

The 75 MHz IF circuit also includes the 75 MHz crystal IF filter, receive path (Q24) and transmit path (Q23) amplifiers, and the switching elements between them.

3.7.3 Control Section

The control section of the radio is based on Motorola HC11 microprocessor and peripheral components, such as ROM, RAM, SLIC and others. For a detailed description of the control section and its operation, refer to paragraph 4 – Control Functions.

4. CONTROL FUNCTIONS

(See Figure 3.)

4.1 GENERAL

The radio's Central Processing and Control unit is located on the S board. It includes the HC11 microprocessor, RAM and EPROM memories and SLIC (I/O Controller) device.

Some of the control devices are located on the A board and are connected to the S board via serial line and discrete control lines.

The following description is based on Figure 3, which shows the main control lines. For clarification and consistency, the following rules were observed regarding the designation of the control lines:

- If the control line performs a function with a descriptive name (i.e: Reset, USB/LSB, etc.) this name will be adopted as the name of the line. If not, the line will be designated by the SLIC or microprocessor pin to which it is connected.
- The names of the SLIC ports are written in Figure 3, and in the description in standard notation. For example, port I-7 is designated as PI7.
- Figure 3 is a block diagram which functionally describes the important blocks and their connections. To maintain clarification not all connections were drawn. In these cases, only the origin and the end of each line are shown.

4.1.1 Getting Keyboard Data

The Processing and Control unit gets the keyboard data by scanning a 4x3 virtual matrix consisting of decoded lines of the "real" keyboard matrix (the decoder of the real keyboard matrix is located on the C board).

The four columns of the virtual matrix are periodically addressed by four SLIC outputs PH0 to PH3. These ports may be either input or output ports. For this utility they are defined as input ports. At that time the three rows are checked by three lines terminated at the SLIC ports, PG0 to PG2.

4.1.2 Writing to the Display

The same lines that check the virtual matrix columns (PH0 to PH3) are used for writing to the display. In this mode the SLIC uses these lines as output lines. The SLIC lines, PG0 to PG3, show 0 at that time, causing the column lines to be isolated from the write-to-display lines. The data is serially transferred to the display and encoded to the appropriate LCD segments by two display drivers located on the C board. The functions of the writing lines are detailed below.

Line	Function
PH0	Defines whether the data on the other lines is display or encoder command data.
PH1	Synchronizes data line in display driver 2.
PH2	Synchronizes data line in display driver 1.
PH3	Serial data line.

4.1.3 Synthesizer Control

The lines which control the PLL devices in the synthesizer circuit are detailed below.

Line	Function
MOSI	Transfers data to PLL devices.
SCK	Transfers clock to PLL devices.
PG4	Latches data in PLL1.
PG5	Latches data in PLL2.
PH4	Latches data in PLL3 (PLL3 is located on the A board).

4.1.4 Digital Selective Calling

The lines, which are used in digital selective calling, perform the following functions:

a. Switching-in the received audio by making PE0 'low' for low gain channel selection, and PE1 'low' for high gain channel selection (these two channels are located on the audio filters' hybrid).

b. Setting the radio in transmit mode by making PA3 (HC11 output) 'high'.

c. Generating the audio tone to be transmitted by PWM switching of PA5.

d. Extinguishing the MON LED and performing audio mute, by making PA7 'low' (and vice versa).

e. Alert tone is performed by raising PA6 to 'high', producing the tone by PWM switching of PA5 and setting the radio in transmit mode by raising PA3 to 'high'.

f. External alarm is performed by raising PSI DATA OUT (SLIC output) to 'high'.

For a detailed description of the digital selective calling, refer to section 4 of this manual – Digital Selective Calling.

4.1.5 Computer Interface

The HC11 lines, TXD and RXD, are used for communication with external devices, when the computer interface option is used.

4.1.6 SPI Communication Lines

The MOSI and SCK lines are used for loading divide coefficients to the PLL integrated circuits. The MOSI lines carry the data and the SCK line is the clock.

The MOSI and SCK lines are also used to push serial data to the shift registers located on the A board.

The target element to be loaded by the MOSI line (synchronized by the SCK line) is as follows:

Target element	Pointing (SLIC) Lines
PLL1	PG4
PLL2	PG5
PLL3	PH4
Shift Registers	SPI CLKOUT

The MOSI, MISO, and SCK lines are transferred out of the board for optional communication with other microprocessors (in such cases the HC11 microprocessor is the 'master').

To complete the communication protocol, two other ports are also transferred out of the board: out port PG6 is used to signal to the "outer" world that the internal microprocessor is busy with internal SPI communication. PG6 is 'high' if the microprocessor is busy, and vice versa.

4.1.7 CW Transmission

When the morse key is pressed, the SLIC in port P17 goes 'low'. The Processing and Control unit detects the change to 'low', and performs the following steps:

a. Sets the radio in transmit mode by making PA3 (HC11 output) 'high'.

b. Generates a 900 Hz tone (square wave) at PA5 (HC11 output).

c. Switches the 900 Hz tone to the sidetone line by making PA6 (HC11 output) 'high'.

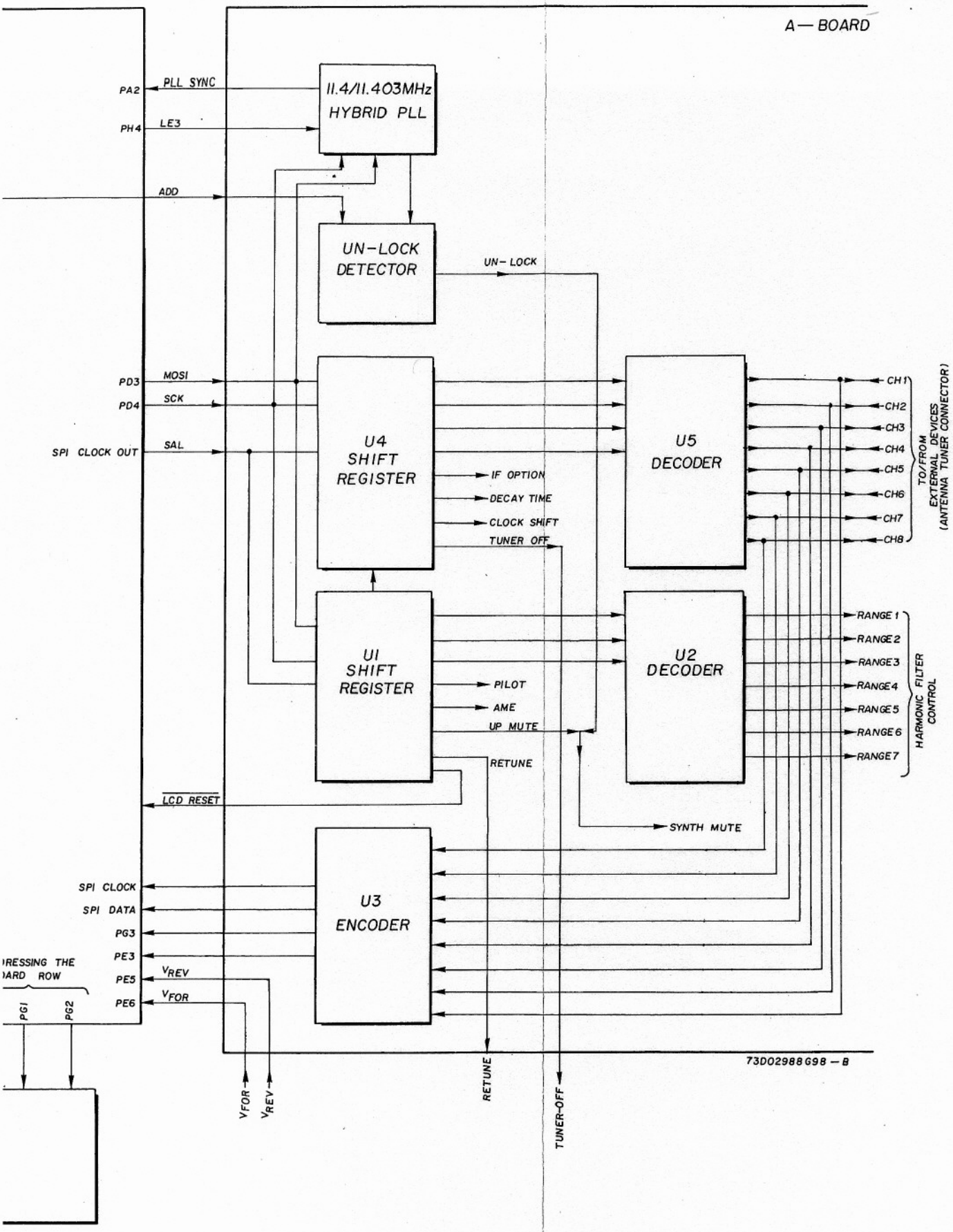
When the morse key is opened, port PA3 stays 'high' (the radio stays in transmit mode), and the Processing and Control unit stops generating the 900 Hz tone.

If the morse key is left open for longer than T sec (where T is the 150 msec or 500 msec CW PTT delay), the Processing and Control unit performs the following steps:

a. Ends transmission (PA3 goes 'low').

b. Ends output power limitation.

c. Inhibits sidetone (PA6 goes 'low').


A — BOARD
PA2
PLL SYNC
11.4/11.403MHz
HYBRID PLL
PH4
LE3
ADD
UN-LOCK
DETECTOR
UN- LOCK
PD3
MOSI
PD4
SCK
SPI CLOCK OUT
SAL
U4
SHIFT
REGISTER
IF OPTION
DECAY TIME
CLOCK SHIFT
TUNER OFF
U5
DECODER
CH1
CH2
CH3
CH4
CH5
CH6
CH7
CH8
TO/FROM
EXTERNAL DEVICES
(ANTENNA TUNER CONNECTOR)
UI
SHIFT
REGISTER
PILOT
AME
UP MUTE
RETUNE
U2
DECODER
RANGE 1
RANGE 2
RANGE 3
RANGE 4
RANGE 5
RANGE 6
RANGE 7
HARMONIC FILTER
CONTROL
LCD RESET
SYNTH MUTE
SPI CLOCK
SPI DATA
PG3
PE3
PE5
PE6
VREV
VFOR
U3
ENCODER
PG1
PG2
73D02988G98 — B
VFOR
VREV
RETUNE
TUNER-OFF

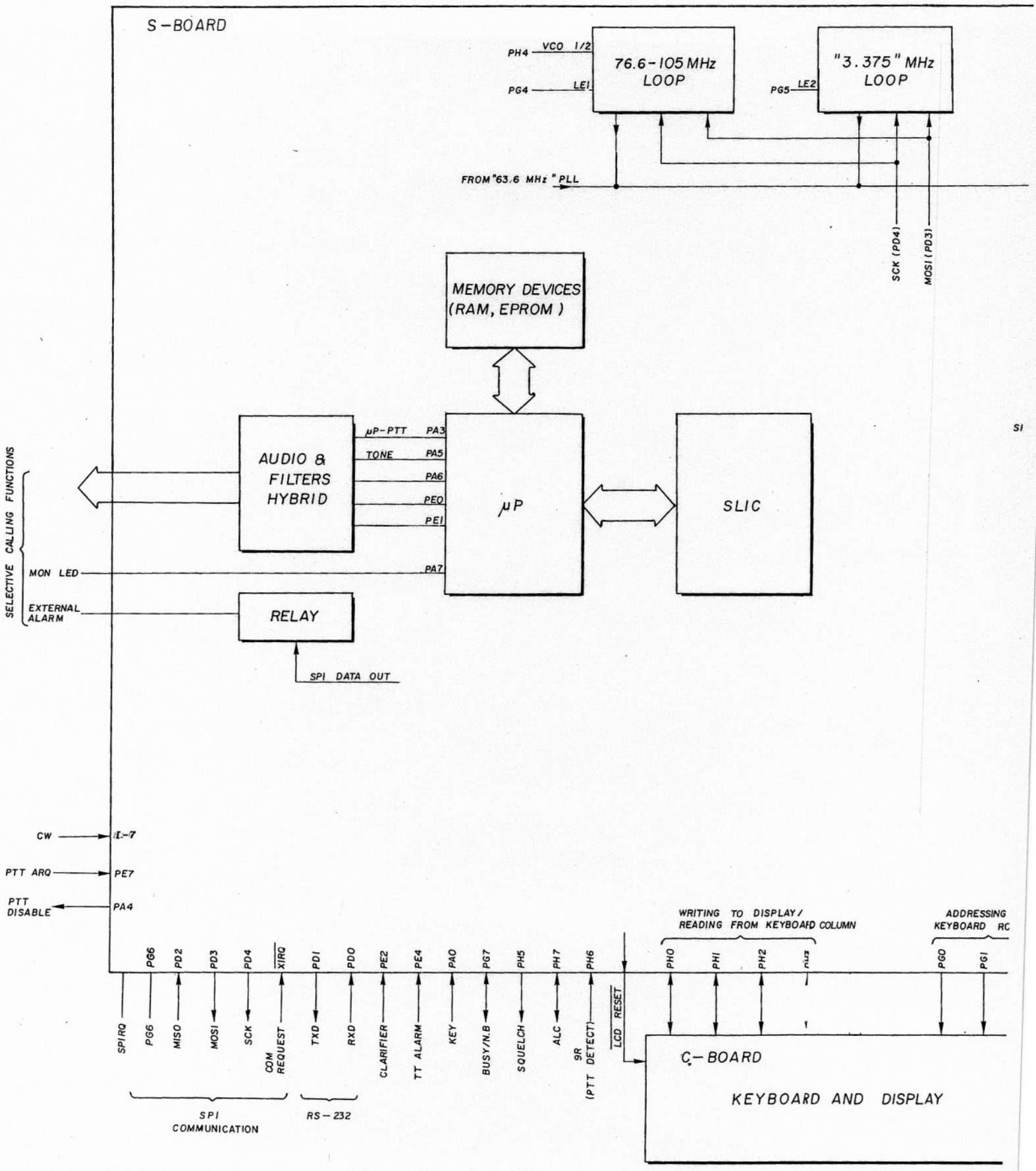


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Figure 3. Control Fu

4.1.8 Audio Monitoring

The operator can override the squelch and/or DSC mute and hear the audio using an audio monitor function. The radio has two types of monitor functions:

- A monitor function which affects both the squelch and DSC mute. This function is activated either by the MON signal from the auxiliary connector pin 1,or by the signal from the microphone connector pin 5. Both these signals are tied on the "A" board to pin 10 of encoder U3. The Central Processing and Control Unit receives the encoded data from the encoder and identifies the monitor request. It then opens the audio path by deactivating either the SQUELCH signal (microprocessor PH5 port) if the squelch mute is on, or the SYNTH MUTE signal (via the "A" board), if the DSC mute is on.

- A monitor function which affects only the DSC mute. The operator activates this function by pressing the [MON] key on the front panel. The Central Processing and Control Unit receives the keyboard status and identifies the monitor request; it then opens the audio path by deactivating the SYNTH MUTE signal (via the "A" board) and extinguishes the MON LED by a command from port PA7.

4.1.9 Squelch

The Processing and Control unit activates/deactivates the squelch circuit according to the position of the squelch key: each press toggles between SQ ON and SQ OFF. The squelch is controlled by the PH5 line of the SLIC.

4.1.10 Noise Blanker Option

The Processing and Control unit activates/deactivates the NB (Noise Blanker) circuit according to the position of the NB key: each press toggles between NB ON and NB OFF.

The NB option circuit, located on the A board, is activated by line PG7 (SLIC port). For NB ON PG7 is 'high' and for NB OFF – 'low'.

4.1.11 BUSY Flag

The PG7 line, normally used as the output line for NB control, may be changed to an input line which checks the display driver BUSY flag. When the drivers' registers are full, the BUSY flag stops the Processing and Control unit from sending data to the drivers until they are empty again.

4.1.12 Access Inhibit

The Processing and Control unit enables/inhibits programming access according to the position of the programming key located on the front panel. When the key is switched on, input line PA0 is 'low' and programming is enabled. When the key is switched off, input line PA0 is 'high' and programming is inhibited.

4.1.13 Sensing the PTT

When PTT is activated, the 9R line, originated in the B board, goes 'low'. The Processing and Control unit senses the 9R line through input line PA1 (HC11 port), thus detecting when PTT is pressed.

4.1.14 V_{FWD}, V_{REV} Lines

These lines, originated in the harmonic filter, carry 0-to-3.5 VDC proportional to the forward and reflected power at the harmonic filter output. These lines are fed to the Processing and Control unit A/D inputs PE5 and PE6 (HC11 ports). The forward and reflected power data is used to display the power bars on the LCD.

4.1.15 Clarifier

This function is controlled by a potentiometer on the front panel. The potentiometer supplies a DC voltage proportional to the desired frequency correction. The DC voltage is fed to the HC11 microprocessor A/D input PE5, and translated to new coefficients for the 11.4 MHz PLL (in receive mode only). As a result, the audio frequency is changed.

4.1.16 USB/LSB

Pressing the USB/LSB key on the front panel toggles between USB and LSB modes. When the Processing and Control unit detects a change request, an appropriate command is sent to the 11.4 MHz and 3.375 MHz PLLs to perform the necessary frequency shifts.

4.2 CONTROL FUNCTIONS VIA THE SERIAL LINE

As above mentioned, the Central Processing and Control unit controls some of the radio's functions via the serial line. This line loads with the current control status two shift registers that are located on the A board. The next functions are controlled by the output of these shift registers.

4.2.1 Harmonic Filter Control

The harmonic filter is controlled by three outputs of shift register U1. These outputs are decoded to one of seven lines. The harmonic filter ranges and the appro-

priate shift register outputs are detailed in the following table:

Shift Register Outputs	Range Frequency (kHz)	Q0	Q1	Q2
1	1600.0– 2429.9	0	1	1
2	2430.0– 3699.9	0	0	0
3	3700.0– 5599.9	1	0	0
4	5600.0–8499.9	0	1	0
5	8500.0–12999.9	1	1	0
6	13000.0–19799.9	0	0	1
7	19800.0–30000.0	1	0	1

4.2.2 Carrier Reinsertion

The carrier reinsertion mode (AME, PILOT) is controlled by two outputs of shift register U1. The Central Processing and Control unit reads the required mode (from the keyboard) and accordingly changes the status of the shift register outputs AME and PILOT, as detailed below:

AME (Q4)	PILOT (Q5)	MODE
0	0	AME
1	1	PILOT
1	0	SSB (No insertion)

4.2.3 Retune

Whenever the frequency or a preselected channel is changed, or when the [ENTER] key is pressed, the Central Processing and Control unit initiates a retune pulse for 450 msec. This is accomplished by changing twice the status of the shift register U1 output Q_D via the serial line. The RETUNE control goes 'low' for 450 msec.

4.2.4 Up-Mute

This line is used to disable the RF power amplifier and to mute the audio. Whenever the microprocessor "decides" to mute the radio it changes the status of the shift register U1 output Q_G via the serial line, thus activating the Up-Mute line (the line goes 'low').

4.2.5 LCD Reset

Whenever the display's drivers should be reset, the microprocessor changes the status of the shift register U1 output Q_H via the serial line, thus activating the LCD RESET control line (the line goes 'low').

4.2.6 Controlling External Devices

The Processing and Control unit can initiate control of one of eight external devices through an external connector on the rear panel J11. This is done by four outputs (Q_A, Q_B, Q_C, and Q_D) of shift register U4 that are decoded to 1 of 10 by decoder U5 (two decoded outputs are not used).

4.2.7 SP Optional IF Filter

The selection of optional IF filter is done via the shift register output: 'IF Option'. When the selected channel defines the special 'IF Option', the microprocessor changes the status of shift register U4 output Q_E via the serial line, thus activating the IF OPTION control line (the line goes 'high').

4.2.8 RGC Decay Time

When the radio is operated in a mode which requires fast RGC decay time (DSC-SCAN), the microprocessor changes the status of shift register U4 output Q_F via the serial line, thus activating the RGC DECAY TIME control line (the line goes 'high').

4.3 MISCELLANEOUS CONTROL FUNCTIONS

4.3.1 PLL Sync

This line is used to synchronize the data loading to the 11.4 MHz PLL hybrids with the PLL operation cycle.

4.3.2 SYNTH Mute

This line is a summation of the Up-Mute and Unlock lines as shown in figure 4 (refer also to paragraph 4.2.4 – Up-Mute, and paragraph 4.3.5 – Unlock).

4.3.3 Channel Selection

One of eight preset channels can be selected by pulling down the channel line of connector J11 on the rear of the PA module. The channel lines arrive at the A board and are encoded to four input lines as shown in the

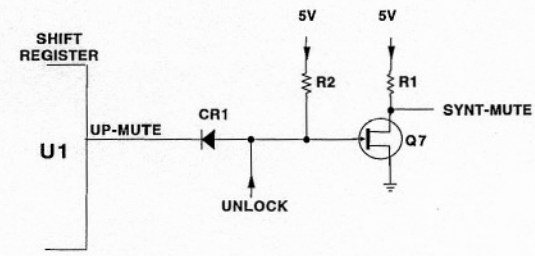

Figure 4. Synthesizer Mute Circuit

following table. These four lines are transferred from the A board to the S board.

Channel	Encoded Lines			
	SPI CLK	SPI DATA	PG3 IN	PE3 IN
1	1	1	1	0
2	1	1	0	1
3	1	1	0	1
4	1	0	1	1
5	1	0	1	0
6	1	0	0	1
7	1	0	0	0
8	0	1	1	1

NOTE

The SPI CLK IN and SPI DATA IN lines are used here, as encoder output lines, and not as the SPI lines of the radio.

4.3.4 ADD

The ADD line is the summation of the OUT-OF-LOCK alert lines of the three PLLs, located on the S board. This line is transferred to the A board.

4.3.5 Unlock

The Unlock line is functionally a sum of the four PLLs OUT-OF-LOCK lines. The summation is accomplished in the A board and enters an Unlock detector circuit. The output of this circuit is the UNLOCK control line.